ABSTRACT

An exemplary sensing circuit comprises a first transistor connected to a first node, where a target memory cell has a drain capable of being connected to the first node through a selection circuit during a read operation involving the target memory cell. The sensing circuit further comprises a decouple circuit which is connected to the first transistor. The decouple circuit includes a second transistor having a gate coupled to a gate of the first transistor. The decouple circuit further has a decouple coefficient (N) greater than 1. The drain of the second transistor is connected at a second node to a reference voltage through a bias resistor. With the arrangement, the drain of the second transistor generates a sense amp input voltage at the second node such that the sense amp input voltage is decoupled from the first node.

Figure 2 should accompany the Abstract.